Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-28. (canceled)

29. (currently amended) A method, comprising:

receiving, at a bridge device, a read request across an expansion bus from an expansion device to a portion of a system memory predetermined to have descriptor addresses;

issuing a read request from the bridge device across a system bus to ~~a portion of a system memory predetermined to have~~ fetch the descriptor addresses ~~associated with the read request~~ from the system memory;

receiving descriptor blocks including descriptor data at the bridge device across the system bus, wherein the descriptor data includes a transmit size of transmit data from the system memory to the expansion device, a location of the transmit data, and an address of the transmit data, and wherein the transmit size indicates an amount of data that the bridge device may pre-fetch from the system memory for the expansion device such that requests for the transmit data from the expansion device are handled entirely at the bridge device without involving the system memory;

storing the descriptor data in a memory on the bridge;

transmitting the descriptor blocks from the bridge device to the expansion device across the expansion bus;

receiving, at the bridge device, a read request from the expansion device for at least a portion of the transmit data, wherein the read request includes a read request address;

searching the memory on the bridge for the read request address; and

if the read request address is located in the memory on the bridge, fetching the portion of the transmit data requested and prefetching any remaining transmit data to match the transmit size by the bridge device, such that any subsequent request for the prefetched transmit data from the expansion device is handled at the bridge device without involving the system memory.

30. (previously presented) The method of claim 29, wherein storing the descriptor data comprises storing the descriptor data in a hash table.

31. (previously presented) The method of claim 30, wherein searching the memory on the bridge further comprises searching the hash table using a read request address as a key.

32. (previously presented) The method of claim 29, the method comprising prefetching the transmit data by cacheline, if the read request address is not locating in the memory on the bridge.

33. (previously presented) The method of claim 29, wherein storing the descriptor data comprises:

determining that the memory on the bridge is full;

discarding an oldest descriptor in the memory on the bridge; and

storing the descriptor in the memory on the bridge.

34. (currently amended) A processor having software that causes the processor to:

receive, at a bridge device, a read request across an expansion bus from an expansion device to a portion of a system memory predetermined to have descriptor addresses;

issue a read request from the bridge device across a system bus to ~~a portion of a system memory predetermined to have~~ fetch the descriptor addresses ~~associated with the read request~~ from the system memory;

receive descriptor blocks including descriptor data at the bridge device across the system bus, wherein the descriptor data includes a transmit size of transmit data from the system memory to the expansion device, a location of the transmit data, and an address of the transmit data, and wherein the transmit size indicates an amount of data that the bridge device may pre-fetch from the system memory for the expansion device such that requests for the transmit data from the expansion device can be handled entirely at the bridge device without involving the system memory;

store the descriptor data in a memory on the bridge;

transmit the descriptor blocks from the bridge device to the expansion device across the expansion bus;

receive, at the bridge device, a read request from the expansion device for at least a portion of the transmit data, wherein the read request includes a read request address;

search the memory on the bridge for the read request address; and

if the read request address is located in the memory on the bridge, fetch the portion of the transmit data requested and prefetch any remaining transmit data to match the transmit size by

the bridge device, such that any subsequent request for the prefetched transmit data from the expansion device is handled at the bridge device without involving the system memory.

35. (previously presented) The processor of claim 34, the software causing the processor to store the descriptor data comprises storing the descriptor data in a hash table.

36. (previously presented) The processor of claim 34, the software causing the processor to search the memory on the bridge further comprises searching the hash table using a read request address as a key.

37. (previously presented) The processor of claim 34, the software causing the processor to prefetch the transmit data by cacheline, if the read request address is not locating in the memory on the bridge.

38. (currently amended) A bridge device, comprising:

a first port to allow the device to communicate with other devices on an expansion bus;

a second port to allow the device to communicate with devices on a second bus;

a memory to store data; and

a processing element to:

receive, at a bridge device, a read request from an expansion device to a portion of a system memory predetermined to have descriptor addresses;

issue a read request from the bridge device across a system bus to ~~a portion of a system memory predetermined to have~~ fetch the descriptor addresses ~~associated with the read request~~ from the system memory;

receive descriptor blocks including descriptor data, wherein the descriptor data includes a transmit size of transmit data from the system memory to the expansion device, a location of the transmit data, and an address of the transmit data, and wherein the transmit size indicates an amount of data that the bridge device may pre-fetch from the system memory for the expansion device such that requests for the transmit data from the expansion device can be handled entirely at the bridge device without involving the system memory;

store the descriptor data in a memory on the bridge;

transmit the descriptor blocks from the bridge device to the expansion device;

receive a read request from the expansion device for at least a portion of the transmit data, wherein the read request includes a read request address;

search the memory on the bridge for the read request address; and

if the read request address is located in the memory on the bridge, fetch the portion of the transmit data requested and prefetch any remaining transmit data to match the transmit size, such that any subsequent request for the prefetched transmit data from the expansion device is handled at the bridge device without involving the system memory.

39. (previously presented) The device of claim 38, the processing element to store the descriptor data comprises storing the descriptor data in a hash table.

40. (previously presented) The device of claim 38, the processing element to search the memory on the bridge further comprises searching the hash table using a read request address as a key.

41. (previously presented) The device of claim 38, the processing element to prefetch the transmit data by cacheline, if the read request address is not locating in the memory on the bridge.

42. (currently amended) A bridge device, comprising:

a means for allowing the device to communicate with other devices on an expansion bus;

a means for allowing the device to communicate with devices on a second bus;

a means for storing data; and

a means for:

receiving, at a bridge device, a read request from an expansion device to a portion of a system memory predetermined to have descriptor addresses;

issuing a read request from the bridge device across a system bus to ~~a portion of a system memory predetermined to have~~ fetch the descriptor addresses ~~associated with the read request~~ from the system memory

receiving descriptor blocks including descriptor data, wherein the descriptor data includes a transmit size of transmit data from the system memory to the expansion device, a location of the transmit data, and an address of the transmit data, and wherein the transmit size indicates an amount of data that the bridge device may pre-fetch from the system memory for the

expansion device such that requests for the transmit data from the expansion device can be handled entirely at the bridge device without involving the system memory;

storing the descriptor data in a memory on the bridge;

transmitting the descriptor blocks from the bridge device to the expansion device;

receiving a read request from the expansion device for at least a portion of the transmit data, wherein the read request includes a read request address;

searching the memory on the bridge for the read request address; and

if the read request address is located in the memory on the bridge, fetching the portion of the transmit data requested and prefetching any remaining transmit data to match the transmit size, such that any subsequent request for the prefetched transmit data from the expansion device is handled at the bridge device without involving the system memory.